13. (Amended) A non-volatile memory of a type including an array of memory cells that individually has a charge storing dielectric material positioned between a conductive gate electrode and a surface of a substrate within a semi-conducting channel that extends across the surface between source and drain regions, comprising:

programming means including voltage sources connectable with the gates, sources and drains for transferring charge to at least two defined regions of the charge storing dielectric of individual addressed ones of the memory cells by one of channel hot-electron injection or source-side injection to levels that adjust thresholds of each of the at least two defined portions of their individual channels to one of more than two threshold levels corresponding to the data being programmed, thereby to store more than one bit of such data in each of the at least two defined regions of the dielectric storage material of individual ones of the cells, and

reading means including voltage sources and sense amplifiers connectable with the gates, sources and drains of individual cells for monitoring a level of current passing through the addressed cells between their source and drain regions in order to measure the programmed one of more than two threshold levels of each of the at least two defined regions of the individual cells.

15. (Amended) The memory of claim 13, wherein the charge storage dielectric includes silicon nitride.

16. (Amended) The memory of claim 13, wherein the charge storage dielectric includes silicon rich silicon dioxide.

17. (Amended) The memory of claim 13, wherein said more than two defined ranges includes exactly four ranges of charge.

18. (Amended) The memory of claim 13, wherein said more than two defined ranges includes more than four ranges of charge.

19. (Amended) A non-volatile memory system, comprising:

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an array of memory cells, wherein the individual memory cells include:

a channel having a length extending between source and drain regions within a substrate surface,

at least first and second conductive gates positioned over different portions of the channel along its length, and

at least first and second storage elements of dielectric charge trapping material sandwiched between respective ones of said at least first and second control gates and said substrate,

a programming circuit including a source of voltages connectable to the source and drain regions and to at least first and second gates of addressed cells to cause electrons to be transferred from the substrate into said at least first and second storage elements by channel hot-electron injection or source-side injection to a storage level according to data being programmed, and

a reading circuit including sense amplifiers connectable to at least one of the source and drain regions of addressed cells for determining the storage level of each of said at least first and second storage elements including monitoring a level of current passing through the addressed cells between the source and drain regions.

20. (Amended) The memory system of claim 19, wherein said individual memory cells have their at least first and second storage elements formed from a layer of charge trapping material extending continuously across the length of the channel between the source and drain regions.

21. (Amended) The memory system of claim 19, wherein the individual memory cells additionally include a third control gate positioned between said at least first and second storage elements along the length of the channel and coupled with the channel through a a layer of dielectric sandwiched therebetween.

22. (Amended) The memory system of any one of claims 19 - 21, wherein the programming circuit includes a source of voltages that causes electrons to be transferred into each of said at least first and second storage elements to one of more than

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two defined storage levels according to more than one bit of data being stored, and wherein the reading circuit includes sense amplifiers connectable to at least the source or the drain for determining the storage levels of one of more than two defined ranges stored in each of said at least first and second charge storage elements.

23. (Amended) A non-volatile memory, comprising:

elongated source and drain regions formed in a semiconductor substrate with their lengths extending in a first direction thereacross and being spaced apart in a second direction, the first and second directions being perpendicular to each other, thereby defining memory cell channels in the substrate between adjacent diffusions,

conductive control gates having lengths extending in the first direction, being positioned in the second direction over channel regions immediately adjacent the diffusions and being spaced apart in the second direction over an intermediate region of the cell channels,

dielectric charge storage material positioned at least between the control gates and a surface of the substrate within the memory cell channels, thereby to provide at least two charge storage regions in the dielectric charge storage material under the control gates in the memory cell channels,

conductive word lines having lengths extending in the second direction and being spaced apart in the first direction, the word lines further being positioned over the control gates and extending therebetween over the intermediate channel regions,

a programming circuit including a source of programming voltages connectable to the source and drain regions, control gates and word lines for adding charge by channel hot-electron injection or source-side injection to the charge storage regions of the dielectric storage material to a storage level according to data being stored, and

a reading circuit including sense amplifiers connectable to at least the source and drain regions for determining the storage level of the individual charge storage regions by monitoring a level of current passing through the individual cells between the source and drain regions.

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25. (Amended) The non-volatile memory of claim 23, wherein the programming circuit operates to transfer charge into common regions of the individual charge storage elements in more than two defined storage levels according to more than one bit of data being stored therein, and wherein the reading circuit operates to determine the storage levels of one of the more than two defined storage levels, thereby to read more than one bit of data from the individual common regions of the charge storage elements.

Please add the following claims:

26. (New) The memory system of claim 21, wherein said at least first and second gate elements are part of respective at least first and second gate lines that are elongated across the array in a direction perpendicular to the channel lengths of the individual memory cells.

27. (New) The memory system of either of claims 21 or 26, wherein the third control gates of the individual memory cells are recessed into the substrate surface.

28. (New) The memory system of claim 27, wherein the third control gates are part of third gate lines that are elongated across the array in a direction parallel with the channel lengths and over the first and second elongated gates in orthogonal relationship therewith.

29. (New) The memory system of claim 21, wherein the third control gates are part of third gate lines that are elongated across the array in a direction parallel with the channel lengths and over the first and second elongated gates in orthogonal relationship therewith.

30. (New) The memory system of claim 21, wherein third control gate forms a select transistor and the layer of dielectric sandwiched between the third control gate and the channel is a gate oxide.

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31. (New) The memory system of claim 19, wherein only the first and second conductive gates are positioned over the channel along its length, thereby including only respective first and second storage elements of dielectric charge trapping material thereunder, and wherein the first conductive gates of the individual memory cells are part of first gate lines that are elongated across the array in a direction perpendicular to the channel lengths of the individual memory cells, and further wherein the second conductive gates of the individual memory cells are part of second gate lines that are elongated across the array along the channel lengths and over the first gate lines in orthogonal relationship therewith.

32. (New) The memory of claim 23, wherein the word lines are recessed into the substrate surface over the intermediate channel regions.

33. (New) The memory of any one of claims 23, 25 or 32, wherein a layer of gate dielectric is positioned between the word lines and the substrate surface over the intermediate channel regions to form select transistors between the control gates.

34. (New) A non-volatile memory, comprising:

elongated source and drain regions formed in a semiconductor substrate with their lengths extending in a first direction thereacross and being spaced apart in a second direction, the first and second directions being perpendicular to each other,

conductive control lines having lengths extending in the first direction and being positioned in the second direction over a first portion of space between neighboring source and drain regions that is immediately adjacent one of the source and drain regions,

conductive word lines having lengths extending in the second direction and being spaced apart in the first direction, the word lines further being positioned over the control lines and extending over a second portion of the space between neighboring source and drain regions that is immediately adjacent another of the source and drain regions and the first portion,

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dielectric charge storage material positioned between the respective control and word lines and a surface of the substrate within the channel regions, thereby to form dielectric charge storage elements under both of the control and word lines,

a programming circuit including a source of programming voltages connectable to the source and drain regions, control lines and word lines for adding charge by channel hot-electron injection or source-side injection to each of the charge storage elements of the dielectric charge storage material in one of at least two defined charge storage levels according to data being stored, and

a reading circuit including sense amplifiers connectable to at least the source and drain regions for determining said one of at least two defined ranges of charge stored in individual charge storage elements including monitoring a level of current passing through the individual cells between the source and drain regions.

35. (New) The memory of claim 34, wherein the first and second charge storage elements are formed from a layer of the dielectric charge storage material that extends continuously across the substrate at least between neighboring source and drain regions.

36. (New) The memory of claim 34, wherein the programming circuit operates to transfer charge into each of the charge storage elements with more than two defined charge storage levels according to more than one bit of data being stored, and wherein the reading circuit operates to determine the storage levels of one of more than two defined charge storage levels, thereby to read the more than one bit of data being stored.

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